REMARKS

This Amendment and Response is in response to the *Final* Office Action of December 21, 2004, where the Examiner has rejected claims 1, 2, 4-9, 12, 14-18 and 20. By the present amendment, claim 12 has been amended. After the present amendment, claims 1, 2, 4-9, 12, 14-18 and 20 are pending in the present application. Reconsideration and allowance of outstanding claims 1, 2, 4-9, 12, 14-18 and 20 in view of the following remarks are requested.

A. Rejection of Claim 12 under 35 USC §112, ¶ 2

The Examiner has rejected claim 12, under 35 USC §112, ¶ 2, as being indefinite for the usage of the phrase "a reference frame memory for storing and supplying a block of pixels associated with a reference block from a reference frame memory."

By the present amendment, applicant has amended claim 12 to read: "a reference frame memory for storing a block of pixels associated with a reference block." Accordingly, it is respectfully submitted that the Examiner's rejection has been overcome.

B. Rejection of Claims 1, 2, 4-9, 12, 14 and 16-18 under 35 USC §102(b)

The Examiner has rejected claims 1, 2, 4-9, 12, 14 and 16-18, under 35 USC §102(b), as being anticipated by Anesko, et al. (USPN 5,987,178) ("Anesko"). For the reasons stated below, applicant respectfully disagrees.

Applicant respectfully submits that Anesko clearly shows that the pixels that are stored in the 8-bank memory 55 are not rearranged and stored therein. This is made clear by the Examiner's own reference to array control 64, which rotates data in the array 52. In other words, assuming, arguendo, Anesko performs any rearranging of the pixels, such rearrangement occurs after the pixels are read from the 8-bank memory 55. This is a significant difference between claim 1 of the present application and Anesko, where claim 1 of the present application recites: "said NxM pixels are rearranged and stored in the staging memory so as to form P groups each having L pixels such that during each read access cycle all L pixels of a different one of the P groups is read from the staging memory to a temporary memory; wherein each group of L pixels corresponds to a new row or a new column of said block of pixels."

This is because unless the pixels are rearranged and stored in the stage memory, a single read access cannot read all pixels in either a new column or a new row.

As disclosed in Anesko, a parallel read can be made of all the pixels in one row, but not either a row or a column. This can be well understood with a reference to FIG. 4 of the present application, which shows a conventional arrangement of pixels. As shown, one row of pixels can be read in one read access cycle without rearrangement, but sixteen read access cycles (8x16 block) are needed to read all the pixels in one column.

This shortcoming of the conventional approach, such as in Anesko, that can only read the pixels in one read access cycle in a single dimension, has been overcome by the

invention of claim 1, where the pixels can be read in read access cycle in both dimensions (i.e., either a new row or a new column).

Furthermore, the Examiner's statement with respect to COLLADD and COLLCHANGE is noted by applicant; however, its is respectfully submitted that Anesko clearly shows that the column selection is not related to the pixels that are read from the staging memory (i.e. 8-bank memory 55), but the processing element array 52, which merely performs operations on the row pixels that have already been read from the staging memory. Therefore, Anesko does not show that all the pixels in a column can be read in one read access cycle. In other words, in Anesko, the pixels can be read in one read access cycle in one dimension only; whereas, with the invention of claim 1, pixels in the staging memory are rearranged such that the pixels can be read in one read access cycle in either one of the two dimensions (row or column), for example, see FIG. 7a (for reading a column) and FIG. 8 (for reading a row).

Accordingly, it is respectfully submitted that independent claim 1, and its dependent claims 2, 4-9, should be allowed. Further, independent claim 12 has limitations similar to those of claim 1. Therefore, claim 12, and its dependent claims 14 and 16-18, should also be allowed.

C. **Rejection of Claim 15 under 35 USC §103(a)**

The Examiner has rejected claim 15, under 35 USC §103(a), as being unpatentable over Anesko in view of Kalapathy (USPN 5,799,169) ("Kalapathy). It is respectfully submitted that claim 15 should be allowed at least for the same reasons stated above in conjunction with patentability of claim 12.

D. **Rejection of Claim 20 under 35 USC §103(a)**

The Examiner has rejected claim 20, under 35 USC §103(a), as being unpatentable over Anesko in view of Maturi, et al. (USPN 5,731,850) ("Maturi"). It is respectfully submitted that claim 20 should be allowed at least for the same reasons stated above in conjunction with patentability of claim 12.

E. Conclusion

Based on the foregoing reasons, an early Notice of Allowance directed to all claims 1, 2, 4-9, 12, 14-18 and 20 pending in the present application is respectfully requested.

Applicant would like to advise the Examiner of a recent change in the attorneys of record, which is confirmed by the attached Revocation and Power of Attorney. Applicant respectfully requests that all correspondence regarding the present application be made to the address shown below.

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CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being filed by facsimile transmission to United States Patent and Trademark Office at facsimile number (703) 872-9306, on the date stated below.

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